REMARKS

Applicant wishes to thank the Examiner for the courtesies extended to the undersigned during the telephonic interview of October 23, 2002. It was agreed during the interview that Applicant would submit this response.

Applicant adds claims 68-80. Accordingly, claims 14-17 and 53-80 are pending in the present application.

Claims 14-17 and 53-67 stand rejected under 35 U.S.C. §103(a) for obviousness over U.S. Patent No. 5,475,317 to Smith.

Applicant respectfully traverses the rejections and urges allowance of the present application.

Claim 14 recites an *electronic device wafer processing intermediate member* comprising, in part, an electrical interconnect configured to electrically connect an electrical coupling of *an electronic device wafer with an electrical coupling of a chuck*. Claim 14 recites patentable subject matter.

Page 2 of the Office Action states that Fig. 3 discloses a die 2. It is stated on page 2 of the Action that it would have been obvious for one of ordinary skill in the art to recognize that die 2 is an electronic device wafer. Applicant disagrees.

Applicant submits herewith literature from P. Van Zandt, "Microchip Fabrication" (4th ed. 2000). Such clearly illustrates the differences between a wafer and a singulated die to clarify the claimed subject matter and what Smith discloses.

As set forth on page 2 of the Office Action, Smith discloses a singulated bare die tester. As set forth in the Abstract, Smith discloses a reusable test socket for testing

singulated bare die. Smith is related to testing of singulated bare dies. The Smith reference fails to teach or suggest the claimed electrical interconnect configured to electrically connect the electrical coupling of the electronic device wafer as defined in claim 14. Applicant has electronically searched the embodiments of the Detailed Description of Smith and has failed to uncover any wafer teachings. The reference teachings of Smith concerning testing of a singulated bare die in no fair interpretation disclose or suggest limitations of claim 14 concerning an electronic device wafer. Claim 14 is patentable over Smith for at least this reason.

On page 2 of the Action it is stated that it would have been obvious for one of ordinary skill in the art to recognize that die 2 is an electronic device wafer. Applicant disagrees. Indeed, Applicant refers the Examiner to teachings in columns 1 and 2 of the Smith reference which illustrates reasons why die 2 would not be recognized as an electronic device wafer. Teachings spanning from column 1, line 45 to column 2, line 17 discuss the vast differences between testing of a wafer and testing of singulated die. For example, testing of a die only certifies that the die is good at a particular stage in a manufacturing cycle and does not test a completely manufactured die. It is thereafter stated that it is important to test the completely manufactured die because defects can be introduced not only when metallization layers are added but also *when the die is separated from the wafer*. Column 2, lines 10-15 describe structures that are designed to contact a die while it is part of an entire semiconductor wafer and are not intended for testing bare singulated die. Accordingly, it is stated that the structures can not be used to test the overall reliability of the bare die to determine whether the die will work. It is clear that

wafers and die are distinct entities and one of skill in the art would not recognize a die as an electronic device wafer as claimed. The prior art of record fails to teach or suggest positively recited limitations of claim 14 and claim 14 is allowable for at least this reason.

To modify the teachings as alleged in the Office Action would destroy the clearly explained purpose of Smith (cols. 1 and 2) to provide *testing of singulated bare die*. *See In re Fitch*, 972 F.2d 1260, 1265 n.12, 23 USPQ2d 1780, 1783 n.12 (Fed. Cir. 1992) (stating that a proposed modification is inappropriate for an obviousness inquiry when the modification renders the prior art inoperable for its intended purpose). The 103 rejection is improper for at least this additional reason.

Further, the proposed modification or combination of the prior art would require substantial reconstruction or redesign of the reference teachings and/or would change the principle of operation of the prior art. According to the MPEP, the teachings of the combined references are not sufficient to render the claims *prima facie* obvious. MPEP 2143.01(8th ed.) *citing In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The *In re Ratti* court reversed a PTO 103 rejection because the suggested combination of references would require a substantial reconstruction and redesign of the elements shown in the primary reference as well as a change in the basic principle under which the primary reference construction was designed to operate. The obviousness rejection is improper for at least these reasons.

Referring to M.P.E.P. §2143.01 (8th ed.), there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine reference teachings. The mere fact

that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. M.P.E.P. §2143.01 citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Obviousness cannot be established by a combination of references unless there is some motivation in the art to support the combination. See ACH Hospital Systems, Inc. v. Montifiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The motivation for forming the combination must be something other than hindsight reconstruction based on using Applicant's invention as a road map for such a combination. See, e.g., Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990).

Contrary to Federal Circuit case law, the M.P.E.P., and PTO procedure, the Office Action fails to identify any motivation for modifying the Smith teachings to allegedly arrive at the rejection of claim 14. There is no motivation and the 103 rejection of claim 14 is improper for at least this additional reason.

The Federal Circuit recently discussed proper motivation In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002). The Court in *In re Lee* stated the factual inquiry whether to combine references must be through and searching. It must be based on objective evidence of record. The Court in *In re Fritch*, 23 USPQ 2d 1780, 1783 (Fed. Cir. 1992) stated motivation is provided only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art. The Lee Court stated that the Examiner's conclusory statements in the Lee case do not adequately address the issue of motivation. The Court additionally stated that the factual question of motivation is

material to patentability and can not be resolved on subjective belief and unknown authority. The Court also stated that deficiencies of cited references can not be remedied by general conclusions about what is basic knowledge or common sense. The Court further stated that the determination of patentability must be based on evidence. In the instant case, the record is entirely devoid of any evidence of motivation. Given the explicit teachings in columns 1 and 2 of Smith, one would not be motivated to modify the teachings of Smith and the rejection of claim 14 is improper for at least this additional reason. The 103 rejection of claim 14 is improper without the proper motivation and Applicants respectfully request allowance of claim 14 in the next action.

Claim 54 recites a *wafer processing apparatus* comprising an intermediate member comprising, in part, a first surface configured to *support substantially an entirety of an electronic device wafer*, a second electrical coupling adjacent to the second surface and configured to electrically connect with an electrical coupling of a *chuck of the wafer processing apparatus*. Claim 54 recites patentable subject matter.

Smith fails to teach or suggest the intermediate member comprising a first surface configured to support substantially an entirety of an electronic device wafer as claimed. To the contrary, Smith clearly relates to testing of singulated die, distinguishes references pertinent to wafers and illustrates die are not to be considered as wafers. Positively recited limitations of claim 54 are not shown or suggested in Smith and claim 54 is allowable for at least this reason.

Additionally, claim 54 recites a *wafer processing apparatus* and the second electrical coupling is configured to electrically connect with an electrical coupling of *a chuck of the*

wafer processing apparatus. Smith is entirely devoid of any processing apparatus let alone apparatus configured to process wafers. Absolutely no processing teachings of Smith have been identified and Smith clearly relates to disparate teachings regarding testing of singulated bare die. Claim 54 recites additional limitations not shown or suggested in the art and claim 54 is allowable for at least this reason.

Referring to M.P.E.P. §2111.02, if the claimed preamble when read in the context of the entire claim recites limitations of the claim or if the claim preamble is necessary to give life, meaning and vitality to the claim, then the claim preamble should be construed as if in the balance of claim. It is further stated that any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation. The Federal Circuit in *Corning Glassworks vs. Sumitomo Elec. USA, Inc.*, 9 USPQ 2d 1962, 1966 (Fed. Cir. 1989) stated that the determination of whether preamble recitations are structural limitations can be resolved only on review of the entirety of the application to gain an understanding of *what the inventors actually invented and intended to encompass by the claim*. It is clear from the replete teachings of the originally filed specification and figures that aspects of what Applicant has invented include wafer processing apparatus and intermediate members of wafer processing apparatus. Claim 54 positively recites limitations of a wafer processing apparatus which are not shown or suggested in Smith and the rejection over Smith is improper for at least this additional reason. As provided in M.P.E.P. §2111.02, the wafer processing apparatus clearly limits the structure of the claimed invention and must be treated as a claim limitation which is not shown or suggested in the prior art. Claim 54 is allowable for at least this additional reason.

Moreover, there is no motivation to modify the teachings of Smith as alleged in the Office Action and the proposed modification of the Office Action would destroy the purpose of Smith. The rejection of claim 54 is improper these numerous reasons.

The claims which depend from independent claim 54 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

For example, referring to claim 56, it is stated on page 2 of the Office Action that it *appears* that an outwardly exposed surface of coupling 2a of die 2 is substantially coplanar with the surface of the die. Applicant disagrees. Fig. 3 of Smith clearly shows die 2 having bond pads 2a. Bond pads 2a individually have three outwardly exposed surfaces, none of which are substantially coplanar with a surface of die 2 (i.e., two such surfaces are perpendicular to the die surface and the other is spaced from the die surface and clearly provided in a plane not coplanar with a surface of the die). Limitations of claim 56 are not shown or suggested and claim 56 is allowable for at least this reason.

Claim 61 recites a *wafer processing apparatus* comprising, in part, an intermediate member comprising an electrical interconnect configured to electrically connect an electrical coupling of an electronic device *wafer* with an electrical coupling of *a chuck of the wafer processing apparatus*, and the electrical interconnect is configured to communicate electrical signals intermediate the electrical coupling of the *wafer* and the electrical coupling of the chuck. Claim 61 is allowable.

Smith fails to disclose or suggest the intermediate member. One of skill in the art would not construe the die to be a wafer as alleged in the Office Action and the 103

rejection of claim 61 is improper for at least this reason. Smith fails to disclose or suggest a wafer processing apparatus and the rejection of claim 61 is improper for this additional reason. There is no motivation to modify the reference teachings and the proposed modification of the Office Action would destroy the purpose of Smith. The rejection of claim 61 is improper for at these numerous reasons.

The claims which depend from independent claim 61 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Some of the new claims recite aspects relative to processing of a wafer. The new claims are supported by the originally filed application and the specification includes numerous teachings of processing workpieces and wafers. M.P.E.P. 2163.07(a) (8th ed.) provides that by disclosing a device (processing apparatus 10) that inherently performs a function (processing functions) or has a property, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage even though it says nothing explicit concerning it. The application may later be amended to recite the function, theory or advantage without introducing new matter according to the MPEP.

Indeed, page two of the application refers to chemically amplified resists which are utilized in deep ultraviolet (DUV) lithography and small micron geometries. Also on page 2, lines 8-12, it is stated that workpiece temperature and workpiece temperature uniformity are parameters which are closely monitored during wafer and workpiece fabrication. As set forth on page 4 of the specification, exemplary sensors include resistance temperature

devices configured to provide process signals containing process information regarding the electronic device workpiece processing apparatus. As set forth on page 2, lines 22-24, temperature sensors across the surface of a wafer are utilized to provide temperature mapping of a workpiece during processing. On page 7, lines 13-19, it is stated that workpieces typically undergo processing from which subsequent devices are formed. Exemplary workpieces include semiconductor wafers, glass or quartz substrates for flat panel or field emission display devices. It is also stated on page 7 that typical production workpieces are processed and subsequently utilized to form products used in a variety of electronic devices. On page 9, lines 4-8, it is stated that process signals provided by sensors 23 and corresponding to processing conditions of workpiece 21 are received within data gathering device 14. Alterations to processing conditions of apparatus 10 can be changed responsive to the reception of the process signals within device 14. On page 16, lines 7-9, it is stated that chuck 40 is isolated to a greater extent from a processing environment utilized to fabricate or process electronic device workpieces. On page 17, lines 3-6, it is stated that one configuration of apparatus 10 of Fig. 6 enables processing of production workpieces while monitoring processing conditions using calibration workpiece 20. Referring to page 19, lines 12-19, it is stated that layer 28 operates to protect surface 21, sensor 23, and electrical connection 27 from the processing environment including gases, chemicals, plasmas, etc. utilized during processing of electronic device workpieces.

Accordingly, the originally filed specification is replete with exemplary teachings of processing a wafer and providing a workpiece processing apparatus (see reference 10 of

the originally-filed specification). The disclosure of the originally filed specification provides support for the claimed subject matter especially with reference to the disclosed exemplary embodiments of electronic device workpiece processing apparatus 10 and processing of workpieces 20 as described in the originally filed specification. In addition, Applicant refers the Examiner to U.S. Patent Application Serial No. 09/032,184 incorporated into the subject application by reference as set forth on page 3, lines 9-15 of the originally filed specification. Serial No. 09/032,184 includes additional teachings providing support for the new claims.

Applicant submits an Interview Summary and a Supplemental Information Disclosure Statement herewith.

Applicant respectfully requests allowance of all pending claims.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 10/24/02

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Application Serial No. 09/825,664
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Examiner . . . . . V. Nguyen
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Title: "Electronic Device Wafer Processing Intermediate Members and Wafer Processing Apparatuses"

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING REQUEST FO CONTINUED EXAMINATION PRELIMINARY AMENDMENT

I n the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

55. (Amended) The apparatus of claim 54 further comprising the ~~electrical~~ electronic device wafer comprising the electrical coupling configured to electrically connect with the first electrical coupling of the intermediate member.

62. (Amended) The apparatus of claim 61 further comprising the ~~electrical~~ electronic device wafer comprising an electrical coupling configured to electrically connect with the electrical interconnect of the intermediate member.

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